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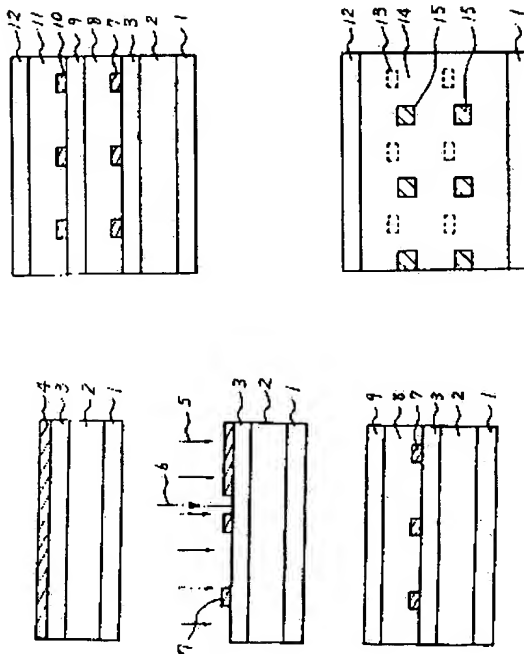
**(54) MANUFACTURE OF  
SEMICONDUCTOR FINE  
STRUCTURE**

(57) Abstract:

**PURPOSE:** To easily manufacture many quantum fine structures by etching Si grown in a single quantum well structure in an arbitrary shape, further growing a semiconductor crystal, then heat treating it to diffuse Si, and partly deleting a semiconductor hetero boundary.

**CONSTITUTION:** A GaAs quantum well layer 3 is grown on the barrier layer 2 of a substrate 1. Then, an Si epitaxial layer 4 is grown. A wafer is fed to an etching chamber, an electron beam 6 is irradiated in an XeF<sub>2</sub> gas, and Si- etched to obtain the remaining pattern 7 of the Si. It is again returned to the single crystal growing chamber, and a barrier layer 8 and a GaAs quantum well layer 9 are grown. Then, the Si is grown, an Si stripe 10 is formed, and a barrier layer 11 and a cap layer 12 are grown. Then, a heat treatment is conducted, and with an Si stripe 13 as a diffusion source the Si is diffused in the quantum well and the barrier layer. The mixed crystal 14 of the quantum well and the barrier layer is formed at a hetero boundary in which the Si is diffused. A buried hetero structure is obtained in a region 15 in which the Si is not diffused.

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